REMARKS

The outstanding Action has been received and duly noted. The above amendments and the following remarks are submitted as a full and complete response thereto.

By this amendment, new claims 12-16 have been added. Support for the newly added claims may be found in FIG. 5 of the present application. Accordingly, claims 5, 8, and 11-16 are submitted for reconsideration.

Amendments to the Specification

The specification has been amended to include a more detailed description of the scanning circuit board 160 (162) shown in FIG. 5.

Claim Rejections

Claims 5, 8 and 11 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-8 of copending Application No. 09/609,651 (*Lin, et al.*).

A terminal disclaimer will be submitted after claims 5, 8 and 11have been reconsidered and placed in condition for allowance.

Claims 5 and 8 stand rejected under 35 U.S.C. §102(e) as being anticipated by *Kinoshita, et al.* (U.S. Patent No. 6,246,385, hereinafter "*Kinoshita*").

Applicant respectfully traverses the above 35 U.S.C. §102(e) rejections of claims 5 and 8 for at least the following reasons.

Kinoshita does not teach, disclose or suggest a first scanning circuit board the same as a second scanning circuit board.

In item 4, the outstanding Action states:

> "Regarding claim 5, referring to Figs. 1-3, Kinoshita teaches a liquid crystal display module, comprising.....a first scanning unit (17A),.....a second scanning unit(17B).....wherein.....the first scanning circuit board is the same the second scanning circuit board.....(see abstract, from col.25, line 1 to col. 26, line 26)"

However, in col. 25, lines 48-51, *Kinoshita* teaches:

> "That is, in FIG. 1, the scanning line left drive circuit 17A and scanning line right drive circuit 17B are distinguished, but identical LSIs for scanning line drive circuit can be used.

Accordingly, the scanning line right drive circuit 17A and scanning line right drive circuit 17B taught by *Kinoshita* are actually LSIs, similar to the first and second scan drivers rather than the first and second scanning units taught in claim 5 of the claimed invention . *Kinoshita* does not teach a first and second scanning circuit board.

Further, even though those skilled in the art will appreciate that the LSIs taught by *Kinoshita* are surely coupled to some circuit boards so that *Kinoshita* implies a first and second scanning unit, *Kinoshita* does not teach that the circuit boards of the two scanning units are the same.

On the contrary, claim 5 of the present application clearly teaches a first and second scanning units respectively comprising a first and second scanning circuit boards, wherein the first and second scanning circuit boards are the same.

For at least this reason, Applicant respectfully submits that Claim 5 is patentable over *Kinoshita*, and that the rejection of Claim 5 should be withdrawn.

Furthermore, Kinoshita does not teach, disclose or suggest first scan drivers and second scan drivers scanning one of scanning lines simultaneously.

In item 4, the outstanding Action states:

> "Regarding claim 5, referring to Figs, 1-3, Kinoshita teaches.....the first scanning unit (17A) and the second scanning unit (17B) drive one of the scanning lines (12) simultaneously;.....(see abstract, from col.25, line 1 to ol.26, line 26)" and
>
> "Regarding claim 8, referring to Figs, 1-3, Kinoshita teaches.....the first scanning unit (17A) and the second scanning unit (17B) drive one of the scanning lines (12) simultaneously;.....(see abstract, from col.25, line 1 to ol.26, line 26)"

However, in col. 25, lines 32-36, *Kinoshita* teaches:

> "...the scanning line left drive circuit 17A scans sequentially from address X1 to XN and from address XN+1 to X2N, and scanning line right drive circuit 17B scans in the reverse direction, from address XN to X1 and from address X2N to XN+1."

Accordingly, in FIG. 1 of *Kinoshita*, the scanning lines (12) are driven in a "downward" sequence by the scanning line left drive circuit 17A and in a "upward"

sequence by the scanning line right drive circuit 17B. That is to say, the scanning line both-end simultaneous driving taught by *Kinoshita* is achieved by driving the scanning lines in two opposite directions respectively on two sides of the panel. Thus, in one single scan period, the scanning line left drive circuit 17A and the scanning line right drive circuit 17B respectively scan two different scanning lines (12), but do not commonly scan a same one of the scanning lines (12).

For at least this reason, Applicant respectfully submits that claims 5 and 8 are patentable over *Kinoshita*, and the rejections of Claim 5 and 8 should be withdrawn.

As for the newly added claim 12, the traces of the signal lines on the first and second circuit boards are clearly taught. These traces are definitely not taught by *Kinoshita*.

For at least this reason, Applicant respectfully submits that Claim 12 is patentable over the cited art, and therefore that Claim 12 is allowable.

Claim 11 stands rejected under 35 U.S.C. §103(a) as being obvious over *Kinoshita* in view of *Sugimoto et al.* (U.S. Patent No. 5,777,610, hereinafter *Sugimoto*).

Applicant respectfully traverses the 35 U.S.C. §103(a) rejection of claim 11 for at least the following reasons.

Neither Kinoshita nor Sugimoto teach, disclose or suggest first scan drivers and second drivers scanning one of scanning lines simultaneously.

As previously stated, in FIG. 1 of *Kinoshita*, the scan drivers on the two sides of the panel respectively scan two different scanning lines. *Sugimoto* does not teach scan drivers on two sides of the panel commonly scanning one of the scanning lines, either.

For at least this reason, Applicant respectfully submits that Claim 11 is patentable over the cited art, and thus that the rejection of Claim 11 should be withdrawn.

Neither Kinoshita nor Sugimoto teach, disclose or suggest a first scanning circuit board the same as a second scanning circuit board, wherein each of the scanning circuit board comprising a first and second scanning interfaces.

As previously stated, *Kinoshita* does not teach a first scanning circuit board the same as a second scanning circuit board. Further, in FIG.4 of *Sugimoto*, the circuit board (14) includes only one single interface coupled to the driver ICs (16). *Sugimoto* teaches neither a scanning circuit board comprising two interfaces nor a first scanning circuit board the same as a second scanning circuit board.

However, in claim 11 of the present application, each of the two scanning circuit boards comprises two interfaces and the two scanning circuit boards are the same.

For at least this reason, Applicant respectfully submits that Claim 11 is patentable over the cited art, and thus that the rejection of Claim 11 should be withdrawn.

Sugimoto does not teach, disclose or suggest an on-board circuit for sending the scanning control signal received to the first or second scanning interfaces both belonging to one circuit board.

In item 6, the outstanding Action states:

> "...referring to Fig. 4, Sugimoto teaches.....an on-board circuit (14) for sending the scanning control signal received to the first or second scanning interfaces..."

However, in FIG. 4 of *Sugimoto*, each of the two on-board circuits (14) sends the scanning control signal to the only one interface of its own. It is impossible for any one of them to send the scanning control signal to one or another interface since only one single interface corresponds to one on-board circuit (14).

On the contrary, in claim 11 of the claimed invention, two scanning interfaces belong to one circuit board so that the on-board circuit of the circuit board sends the scanning control signal to one or another scanning interface.

For at least this reason, Applicant respectfully submits that Claim 11 is patentable over the cited art, and that the rejection of Claim 11 should be withdrawn.

As for the newly added claim 12, the traces of the signal lines on the first and second circuit boards are clearly taught. Definitely, neither *Kinoshita* nor *Sugimoto* teach the signal line traces on the circuit board.

For at least this reason, Applicant respectfully submits that Claim 12 is patentable over the cited art, and thus that Claim 12 is allowable.

Conclusion

For at least the reasons described above, Applicant respectfully submits that claims 5, 8, 11 and 12 are allowable in their present form. Moreover, insofar as claims 5, 8, 11 and 12 are allowable, claims 13, 14, 15 and 16, which depend from claims 5, 8, 11 and 12, respectively, and include every claimed element thereof, are also allowable on their own merits in claiming additional elements not included in claims 5, 8, 11, and 12.

In view of the amendments to the specification and claims and the remarks set forth above distinguishing the claimed invention from the cited prior art references, Applicant submits that the Examiner's rejections have been overcome. It is therefore respectfully requested that the Examiner withdraw the rejections and allow the present claims.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the

telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. The fees for such an extension or any other fees which may be due with respect to this paper, may be charged to Deposit Account No. 50-2394.

Respectfully submitted,

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